Abstract

In a memory system, multiple memory modules (208-211, Figure 2) communicate over a bus (220). Each memory module includes a hub (302, Figure 3) and at least one memory storage unit (304). The hub receives local data (410, Figure 4) from the memory storage units, and downstream data (420) from one or more other memory modules. The hub assembles (718, Figure 7) data to be sent over the bus within a data block structure (440), which is divided into multiple lanes (508-515, Figure 5). An indication is made (612, Figure 6) of where, within the data block structure, a breakpoint will occur in the data being placed on the bus by a first source (e.g., the local or downstream data). Based on the indication, data from a second source (e.g., the downstream or local data) is placed in the remainder of the data block, thus reducing gaps on the bus.

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